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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/997,019	11/28/2001	John Whitman	4294.2US (98-1208.2)	6139

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EXAMINER
KEBEDE, BROOK

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/997,019	Applicant(s) WHITMAN ET AL.	
	Examiner Brook Kebede	Art Unit 2823	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,5,6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2 and 10–22 are rejected under 35 U.S.C. 102(e) as being anticipated by Lu et al. (US/6,146,968).

Re claim 1, Lu et al. disclose a method for preparing a surface of a semiconductor device structure for planarization, comprising: providing a semiconductor device structure (Fig. 3) including at least one recess (110) formed in a surface (not labeled) thereof and a first material layer (112) substantially filling said at least one recess (110) and covering said surface (not labeled), said first material layer (112) having a non-planar surface (i.e., HSG or rugged polysilicon); applying a second material (114) to said first material layer (112); and spreading said second material (114) over said first material layer (112) so as to forming a second material layer (114) having a substantially planar surface without requiring subsequent planarization of said second material (114) (see Figs. 1-5 and Col. 2, lines 48-63).

Re claim 2, as applied to claim 1 above, Lu et al. disclose all the claimed limitation including the limitation wherein said applying said second material (114) comprises applying a stress buffer material (i.e., photoresist) to said first material layer (112) (see Figs. 1-5 and Col. 2, lines 48-63).

Re claim 10, as applied to claim 2 above, Lu et al. disclose all the claimed limitations including the limitation wherein said spreading comprises at least partially filling at least one valley of said first material layer with said stress buffer material while leaving at least one peak of said first material layer substantially uncovered by said stress buffer material (see Figs. 1-5 and Col. 2, lines 48-63).

Re claim 11, as applied to claim 10 above, Lu et al. disclose all the claimed limitations including the limitation planarizing at least said first material layer (see Figs. 1-5 and Col. 2, lines 48-63).

Re claim 12, as applied to claim 11 above, Lu et al. disclose all the claimed limitations including the limitation wherein said planarizing comprises etching at least one region of said first material layer exposed through said stress buffer material with selectivity over said stress buffer material (see Figs. 1-5 and Col. 2, lines 48-63).

Re claim 13, as applied to claim 12 above, Lu et al. disclose all the claimed limitations including the limitation wherein said etching is effected until a surface of said at least one region is in substantially the same plane as a surface of said stress buffer material (see Figs. 1-5 and Col. 2, lines 48-63).

Re claim 14, as applied to claim 13 above, Lu et al. disclose all the claimed limitations including the limitation wherein said planarizing further comprises abrasively planarizing said stress buffer material and said at least one region to expose said surface of said semiconductor device structure adjacent said at least one recess, said surface of said semiconductor device structure and a surface of said first material layer in said at least one recess being located in substantially the same plane following said planarizing (see Figs. 1-5 and Col. 2, lines 48-63).

Re claim 15, as applied to claim 13 above, Lu et al. disclose all the claimed limitations including the limitation wherein said planarizing further comprises concurrently etching said first material layer and said stress buffer material at substantially the same rate so as to expose said surface of said semiconductor device structure adjacent said at least one recess with said surface of said semiconductor device structure and a surface of said first material layer in said at least one recess being located in substantially the same plane following said planarizing (see Figs. 1-5 and Col. 2, lines 48-63).

Re claim 16, as applied to claim 11 above, Lu et al. disclose all the claimed limitations including the limitation wherein said planarizing is effected until said surface of said semiconductor device structure is exposed through said first material layer (see Figs. 1-5 and Col. 2, lines 48-63).

Re claim 17, as applied to claim 16 above, Lu et al. disclose all the claimed limitations including the limitation wherein said etching is effected until a surface of said first material layer in said at least one recess is in substantially the same plane as said surface of said semiconductor device structure (see Figs. 1-5 and Col. 2, lines 48-63).

Re claim 18, as applied to claim 16 above, Lu et al. disclose all the claimed limitations including the limitation removing said stress buffer material from said semiconductor device structure (see Figs. 1-5 and Col. 2, lines 48-63).

Re claim 19, as applied to claim 2 above, Lu et al. disclose all the claimed limitations including the limitation wherein said spreading comprises forming a substantially planar surface over said semiconductor device structure (see Figs. 1-5 and Col. 2, lines 48-63).

Re claim 20, as applied to claim 19 above, Lu et al. disclose all the claimed limitations including the limitation planarizing at least said first material layer (see Figs. 1-5 and Col. 2, lines 48-63).

Re claim 21, as applied to claim 20 above, Lu et al. disclose all the claimed limitations including the limitation wherein said planarizing comprises substantially concurrently abrasively planarizing said stress buffer material and said first material layer to surface of said semiconductor device expose said device structure adjacent said at least one recess, said surface of said semiconductor device structure and a surface of said first material layer in said at least one recess being located in substantially the same plane following said planarizing (see Figs. 1-5 and Col. 2, lines 48-63).

Re claim 22, as applied to claim 20 above, Lu et al. disclose all the claimed limitations including the limitation wherein said planarizing comprises substantially concurrently etching said first material layer and said stress buffer material at substantially the same rate so as to expose said surface of said semiconductor device structure adjacent said at least one recess with said surface of said semiconductor device structure and a surface of said first material layer in said at least one recess being located in substantially the same plane following said planarizing (see Figs. 1-5 and Col. 2, lines 48-63).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 3, 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Lu et al. (US/6,146,968) in view of Yoshihara (US/6,117,486).

Re claims 3-5, as applied to claim 1 above, Lu et al. disclose all the claimed limitations. Although is a well-known process, Lu et al. do not disclose decreasing a rate of the spinning while permitting the material to at least partially cure and gradually increasing the rate of the spinning.

Yoshihara discloses applying the material to the surface of the semiconductor device structure spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning; exposing the material to a soft balling temperature; spinning rate of 1000 and 100 rpm (see Figs. 10 and Col. 13, lines 25-44). As Yoshihara discloses the method provided forming of resist film on the semiconductor wafer at predetermined and uniform thickness.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. reference with spinning the semiconductor device structure both decreasing rate of

spinning and while allowing the material to cure gradually increasing the rate of spinning as taught by Yoshihara because the method would have provided to form a resist film on the semiconductor wafer at predetermined and uniform thickness.

5. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Lu et al. (US/6,146,968) in view of Jenq (US/6,303,430).

Re claims 6 and 7, as applied to claims 1 above, Lu et al. disclose all the claimed limitations. Although it is well-known in the art, Lu et al. do not specifically disclose providing a shallow trench structure.

Jenq disclose a shallow trench isolation structure (22) filled with an oxide film during manufacturing of capacitor structure (see Fig. 6H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Lu et al. reference with shallow trench isolation structure as taught by Jenq because the shallow trench isolation would have provided the device an isolation between the active areas.

6. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Lu et al. (US/6,146,968) in view of Hsich (US/6,228,711).

Re claims 8 and 9, as applied to claim 1 above, Lu et al. disclose all the claimed limitations. Although it is well-known in the art, Lu et al. do not specifically disclose providing dual-damascene structure.

Hsich et al. disclose forming of dual-damascene structure and forming a conductive layer over the dual-damascene structure (see Fig. 3H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Lu et al. reference

with dual-damascene structure as taught by Hsich et al. because, as well-known in the art, the structure would have increased the device density.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Ping (US/6,235,605), Kikuchi et al. (US/6,278,153), and Lou (US/6,417,066) also disclose similar inventive subject matter.

Correspondence

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
February 12, 2003

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800